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REVIEW ARTICLE

Study and Analysis of Low Power Barrel Shifter Using CMOS Technology

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ABSTRACT

Data computing and high-speed digital signal processing rely heavily on bit manipulation, which includes pivot and shift operations. The most common tool for accomplishing these tasks efficiently is the barrel shifter. One potential alternative technology to complementary metal-oxide semiconductors for designing high-speed circuits is nanomagnetic logic (NML) circuits. A combinational circuit is the most common type of nanomagnet circuit now in use. In this study, an in-plane NML-based barrel shifter is developed and produced. Barrel shifters/rotators can be used with 2:1, 4:1, 8:1, etc. multiplexer units to perform shifting and rotating operations independently or simultaneously. The multiplexer unit allows the barrel shifter/rotator to utilize it again, which reduces power consumption. Nanomagnetic logic circuits have never before been suggested. For the RISC processor to run as efficiently as possible, the barrel shifter is an essential component; it rotates and transfers data in both the left and right directions.

Key words: Barrel shifter, cadence, diode free adiabatic logic, double gate MOSFET, LECTOR technique, low power, operating frequency, pass transistor logic, power consumption

INTRODUCTION

In light of the increasing expectations placed on complementary metal-oxide semiconductor (CMOS) scaling and the restrictions that come with it, field-coupled devices represent a potential alternative.[1-8] The new intriguing concepts in beyond-CMOS computing, such as quantum-dot cellular automata (QCA), can produce high-performance systems with reduced power-delay products, simpler interconnections, and larger packing densities. These metal-based QCA circuits have a number of drawbacks that make them impractical for real-world applications, including poor conversion efficiency, low operating temperature, low device production yield, and decoherence. On the other hand, high-performance circuits may be realized at room temperature with the help of nanomagnets.[7,8,11,12] These circuits communicate with one another throughmagnetic dipole interactions that couple the magnetization states of individual nanomagnet domains. The main benefits of circuit design based on nanomagnets are non-volatile memory and the absence of current movement. Nanomagnetic logic (NML) circuits are those that have been built employing controlled field applications and nanomagnets.[13,14] An NML can be either in-plane (iNML) or perpendicular (PNML). There have been several efforts to create and verify NML circuits. The Torino Polytechnic nanotechnology (Topol Nano) tool stands out among the available tools when it comes to validating NML circuits, according to researchers. The Topol Nanotool generates and simulates circuit layouts automatically in iNML. Half adders, full adders, multiplexers, demultiplexers, decoders, ripple carry adders, 32-bit Pentium-4 tree-Adders, ISCAS 85 benchmarks, and systolic multipliers are almost all combinational circuits that have been designed and validated by the tool in the printed word. There has been very little design of sequential circuits in iNML.

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LITERATURE WORK

The authors of Pillmeier (2002)[15] showed how a barrel shifter works in its most fundamental form. They have compared and contrasted barrel shifters based on MUX and mask designs. With the use of Virtuoso software, a fully bespoke 2-bit BS was designed in Agrawal and Mehra[16] utilizing 2 × 1 MUX in CMOS 45 nm technology. They boasted that their pass transistor logic architecture cut power consumption by 76.3% and time delay by 91.77% compared to the standard approach. Using the Xilinx 12.1 ISE software tools, four-bit and eight-bit BS circuits were shown in Maity and Maity.[17] Regarding data shifting and data rotation, Verma and Mehra notes that barrel shifter is really significant. There are a lot of places it can be used. Data shifting simplicity is the primary use case for the barrel shifter. Another option is to use the barrel shifter instead of the arithmetic or logical shifters. The data can be shifted to the right or left, either mathematically or conceptually, when it is rotated, which is useful for applications. The goal is to create a two-bit barrel shifter utilizing CMOS logic, universal gates, and two 2:1 multiplexers (muxes), which are crucial components. Their proposal also includes the more sophisticated 4-bit data shifting variant of the barrel shifter. It details the various design techniques utilized to minimize the circuit's area, power consumption, and size, including conventional cell-based design, semicustom design, and complete custom design, for the barrel shifter. It examines the barrel shifter's area and power utilizing 45 nm technologies and optimizes them.

Patnaik *et al.*[18] When dealing with embedded system hardware register programming, bit-wise operations are crucial. Changing the whole value of a register might be tedious and unattractive when they just need to modify a single bit. This happens rather often. One of the several practical bit operations is bit shifting. Based on their research, they have developed a 32 nm CMOS bit-shifter that can accommodate arithmetic shift, right shift, no-shift, and left-shift operations as needed. Results from the simulations are generated using the SILVACO program Bhardwaj and Khare.[19]

The main characteristics of CMOS technology include low power consumption, small size, and little latency, among others. For the majority of today's embedded systems, these are fundamental design concerns. A major contributor to system power consumption in modern CMOS technology is logic switching. A larger switched load and a higher switching frequency result in a greater power consumption. Bus invert coding and shift invert coding are two prominent methods for minimizing the number of bus transitions in CMOS circuits, which helps to minimize power consumption. Shift invert coding utilizing a barrel shifter is the proposed new method. With this method, less physical labor is required. It has little impact on the system since it operates quickly and uses little electricity. It improves the system's efficiency, which in turn increases the system's precise value. To go a step further, the suggested method generates the coding bits by sending data to the transition block after picking the right selection line. It includes "the implementation of the suggested method using 0.18 micron scalable CMOS technology utilizing the Software tools: Electric version 8.11 and cadence." The power consumption has been minimized by the use of many design elements at every stage of the sub-block implementation.

Sachan *et al.*[20] It is usual practice for general-purpose and integrated digital signal processors to use barrel shifters to manipulate data. Here they take a look at several different ways that barrel shifters may be designed to do the following: shift left arithmetic, rotate right, shift left logical, and shift left. For a range of operand sizes, four distinct barrel shifter designs are showcased and evaluated according to area and delay. Along with the shift or rotate operation, this also looks at methods for identifying zero results, which leads that overflow.

BARREL SHIFTER/ROTATOR CIRCUIT

Shifters

An exact amount of bits can be shifted in a single clock cycle by means of a combinational circuit known as a barrel shifter. It takes a set of control inputs, produces a number of outputs, and has a number of inputs. A multiplexer unit is used to implement the barrel shifter in this study. It is the shift distance that determines how this design links the output of one multiplexer block to the input of the subsequent multiplexer block. To construct a bit barrel shifter, the required number of multiplexer units is determined by, where N is

the number of input bits. Table 1 below lists the shifting operation.

In the Table 1 above, "c" indicates the select or control line set, "a" symbolizes the 8-bit input vector, and "y" represents the 8-bit output vector. An "L" indicates a low state, whereas a "H" indicates a high condition. This work presents an implementation of the barrel shifter circuit using multiplexer units. Figure 1 depicts the barrel shifter's design. Multiplexer units are first developed using CMOS logic and subsequently executed using various low-power designs detailed in section III. A. Rotor in the three-stage 8-bit rotator circuit, 4-bit, 2-bit, and 1-bit rotations is used. Each bit from the input is sent to the output via a rotator circuit, therefore zero-carrying wires are not needed. The stage that is controlled by, on the other hand, uses the connection lines to send low-order data bits to high-order multiplexors. Figure 2 depicts the right rotator design. There are three independent settings for the 8-bit right rotator shown in Figure 2. At the first level, which is controlled by the "b0" control input, it can right-rotate four bits. The second level, which provides two-bit right-rotation, is activated by the "b1" control input. The control input "b2" allows for adjustment of the final level, which provides a one-bit right shift. C. Right shifter and rotator based on multiplexers A right shifter and rotator can be added to the logical right shifter by adding extra multiplexer units. Figure 3 displays the design. The three-tiered operation is also present here. On the bottom level, it can see a single bit of shift/rotate, whereas on the top level, it can see four bits. Starting with a single multiplexor selecting '0' for logical right shifting or 'arithmetic right shifting' to produce S, the process advances. Multiplexors manipulate data by rotating lower bits and moving S when they encounter a block.

Table 1: Shifting operation of 8 bit barrel shifter

c2	c1	c0	y7	y6	y5	y4	y3	y2	y1	y0
L	L	L	a7	a6	a5	a4	a3	a2	a1	a0
L	L	H	a0	a7	a6	a5	a4	a3	a2	a1
L	H	L	a1	a0	a7	a6	a5	a4	a3	a2
L	H	H	a2	a1	a0	a7	a6	a5	a4	a3
H	L	L	a3	a2	a1	a0	a7	a6	a5	a4
H	L	H	a4	a3	a2	a1	a0	a7	a6	a5
H	H	L	a5	a4	a3	a2	a1	a0	a7	a6
H	H	H	a6	a5	a4	a3	a2	a1	a0	a7

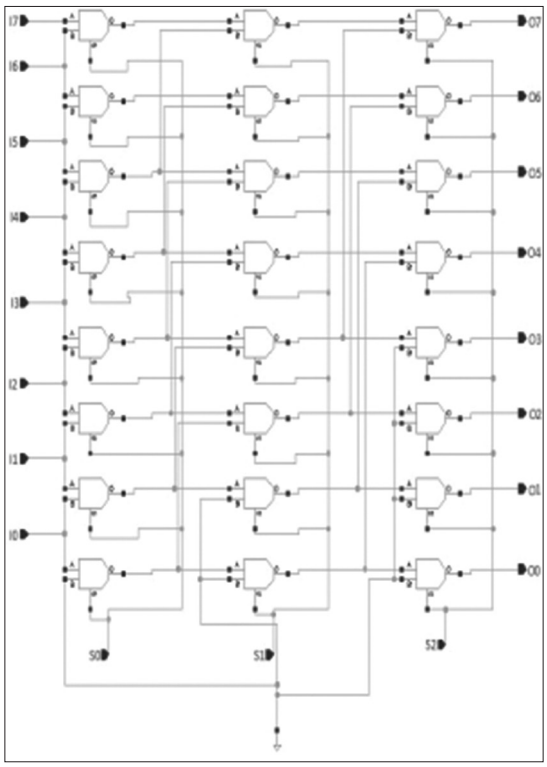

Figure 1: Schematic of 8- bit Barrel shifter

IMPLEMENTING THE BARREL SHIFTER/ROTATOR CIRCUIT

Low Power Techniques

The multiplexer units are responsible for implementing the circuit of the barrel shifter/rotator. The following low-power strategies were used in the design of these multiplexer units. Part A: Logic for Passing Transistors. While with a complementary MOSFET, the primary

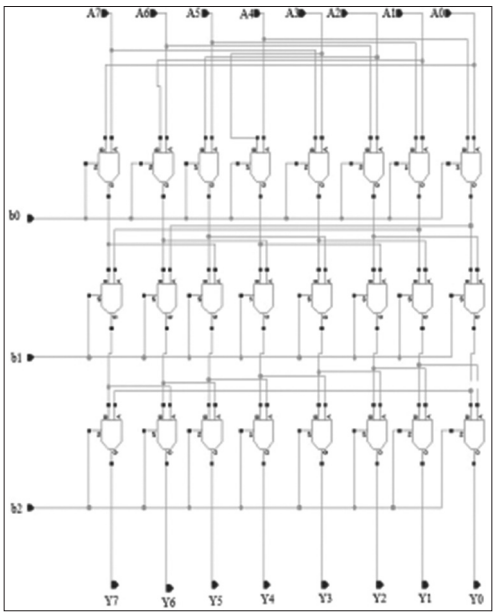

Figure 2: Schematic of 8 right rotator

inputs can only drive the gate terminal, in pass transistor logic, they can drive the source/drain or gate terminals of a MOSFET. Consequently, both area and latency are decreased due to a decrease in the number of transistors employed. As seen in Figure 4, the multiplexer is implemented using pass transistor logic.

LECTOR Technique

Reducing circuit leakage power is the primary goal of the LECTOR approach, which involves connecting the supply and ground through a stack of transistors. A CMOS gate is utilized in this method. It has two leakage control transistors (LCTs) sandwiched between the pull-up and pull-down networks, with the source terminal of one LCT inhibiting the gate terminal of the other. In the setup described above, the cut-off zone of one LCT is used for operation. It can see the procedure. Compared to previous low-power solutions, the multiplexer units developed using the LECTOR methodology in this study display relatively little latency. This section explains the findings of the power and delay calculations.

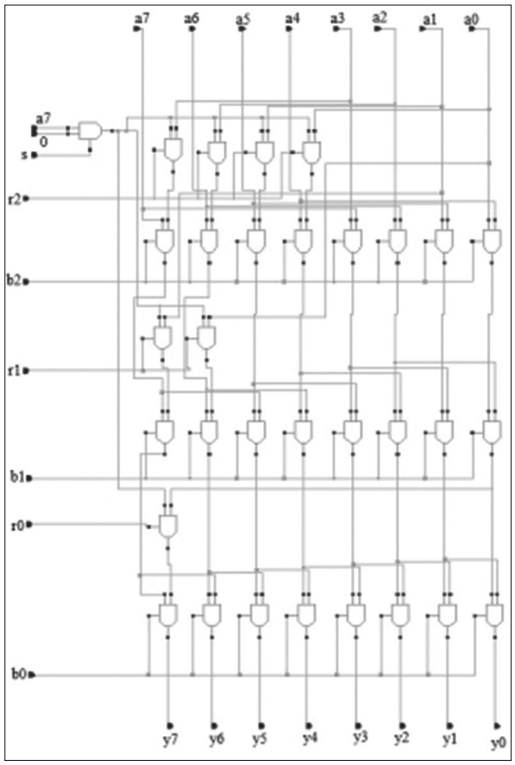

Figure 3: Schematic of 8-bit right shifter/rotator

DFAL Technique

This DFAL method divides the circuit's operation into an evaluation phase and a hold phase, named after the phases of the supply clock signal. Swings increase and Vbar decrease during the assessment phase, and vice versa during the hold phase. When the pull-up network, also known as the PMOS network, is turned on during the evaluation phase, the load capacitance C L is charged, resulting in a high state as the output. When the NMOS transistors are switched on and the pull-down network, also known as the NMOS, is turned on, the load capacitor drains, causing the output logic state to become low. There are no output transitions during the hold phase when the pull-down network is switched on, and C L discharges when the output state is high and the PMOS is turned on. Energy dissipation is decreased as a result of switching because dynamic switching is reduced. In Figure 5, it can see the DFAL logic. When it comes to reducing overall circuit power consumption, the DFAL method is quite effective. Here, this method is used to create the multiplexer units, which are then used to implement the barrel shifter/rotator circuit.

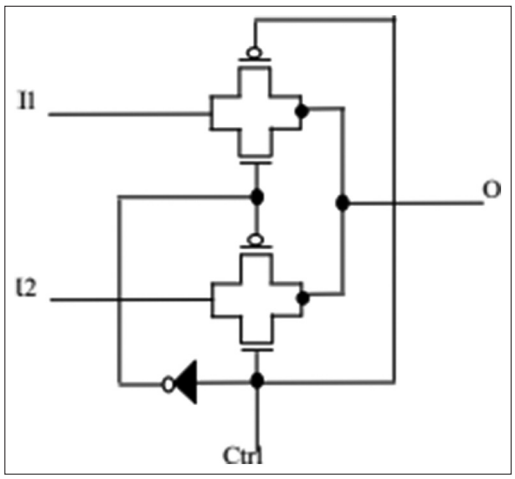

Figure 4: 2:1 Multiplexer employing pass transistor logic

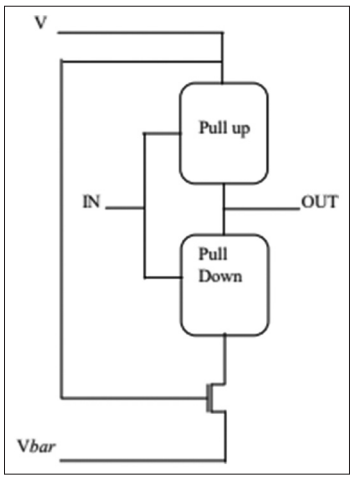

Figure 5: DFAL logic

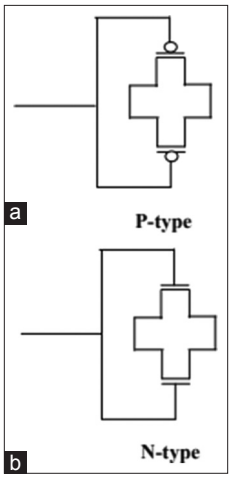

Figure 6: (a and b) Kinds of double-gate MOSFET

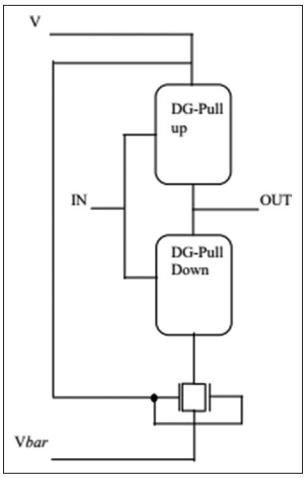

Figure 7: Double gate-DFAL logic

Table 2: Compare the average power and delay of an 8-bit barrel shifter/rotator circuit

Shifter/Rotator Design	Supply Voltage (0.8V)		Supply Voltage (0.7V)		Supply Voltage (0.6V)	
	Power(μW)	Delay(ps)	Power(μW)	Delay(ps)	Power(μW)	Delay(ps)
CMOS	7.228	129.4	7.390	129.4	7.397	129.3
Pass Transistor	5.984	114.6	3.778	114.5	2.547	114.1
LECTOR	1.863	109.4	1.911	109.3	1.885	109.2
DFAL	1.273	129.9	1.202	129.4	1.154	129.7
DG-MOSFET	2.135	74.68	2.043	92.52	2.014	104.2
Proposed Design	1.245	50.42	1.201	50.45	1.147	49.47

Double Gate MOSFET

The majority of low-power circuit designs use the double gate MOSFET construction. A double-gate MOSFET can control its scaled-width channel by use of gates that are attached to either side of the device. It is possible to reduce power consumption and increase performance by individually driving the front gate and back gate of this device. Scalable silicon transistors are another name for double-gate MOSFET devices because of the remarkable control they have over the short-channel effects in their construction.

The symmetrically linked P-type and N-type double gate MOSFETs are illustrated in Figure 6. The two gates of the double-gate MOSFET can be linked to separate voltage sources, making it an asymmetric type. This study also uses this double gate MOSFET approach to create the multiplexer units, which means the barrel shifter/rotator circuit is also used.

Proposed Technique

A novel approach, combining the DFAL method with double-gate MOSFETs, is suggested in this study. There was a considerable improvement in latency and power savings with this novel method. Figure 7 illustrates the reasoning behind the novel method.

Table 2 compares the average power and delay of an 8-bit barrel shifter/rotator across various designs and supply voltages. The "Proposed Design" consistently outperforms all others, achieving the lowest power consumption (1.147–1.245 uW) and significantly reduced delays (around 50 ns), especially benefiting from lower supply voltages.

CONCLUSION

The subthreshold leakage current dissipation of the entire circuit rises with decreasing technology, which in turn impacts the efficiency of the circuit. Therefore, to handle power and delay concerns, it is necessary to enhance the execution of the circuit design. Several methods for designing circuits with little power consumption are detailed in this article, and these methods were used to construct barrel shifter/rotator circuits. To lessen power dissipation in very large-scale integration designs, it has laid down an effective design process. The hybrid circuit outperforms pure CMOS in terms of linear

responsiveness while taking up less space. When compared to the previously published architecture, their approach demonstrates significant power reductions throughout a wide tuning range.

REFERENCES

1. Lent CS, Tougaw PD, Porod W, Bernstein GH. Quantum cellular automata. Nanotechnology 1993;4:49-57.
2. Cowburn RP, Welland ME. Room temperature magnetic quantum cellular automata. Science 2000;287:1466-8.
3. Csaba G, Porod W. Behavior of nanomagnet logic in the presence of thermal noise. In: 2010 14th International Workshop on Computational Electronics. United States: IEEE; 2010. p. 1-4.
4. Niemier MT, Kogge PM. Problems in designing with QCAs: Layout = timing. Int J Circuit Theory Appl 2001;29:49-62.
5. Momenzadeh M, Huang J, Tahoori MB, Lombardi F. On the evaluation of scaling of QCA devices in the presence of defects at manufacturing. IEEE Trans Nanotechnol 2005;4:740-3.
6. Raj M, Gopalakrishnan L, Ko SB. Design and analysis of novel QCA full adder-subtractor. Int J Electron Lett 2021;9:287-300.
7. Panchal V. Designing for longer battery life: Power optimization strategies in modern mobile SOCS. Int J Electr Eng Technol 2025;16:1-17.
8. Chandu HS. Robust control of electrical machines in renewable energy systems: Challenges and solutions. Int J Innov Sci Res Technol 2024;9:594-602.
9. Vacca M, Frache S, Graziano M, Riente F, Turvani G, Roch MR, *et al*. ToPoliNano: Nanomagnet logic circuits design and simulation. In: Lecture Notes in Computer Science. Berlin: Springer; 2014. p. 274-306.
10. Csaba G, Becherer M, Porod W. Development of CAD tools for nanomagnetic logic devices. Int J Circuit Theory Appl 2013;41:634-45.
11. Panchal V. Energy-efficient core design for mobile processors : Balancing power and performance. Int Res J Eng Technol 2024;11:191-201.
12. Chandu HS. A review on CNC machine tool materials and their impact on machining performance. Int J Curr Eng Technol 2024;14:313-9.
13. Patel R. Remote troubleshooting techniques for hardware and control software systems: Challenges and solutions. Int J Res Anal Rev 2024;11:933.
14. Mohammed A, Daou S, Guedoir A, Scinto R, Rajavel V. Fault Management and Design-for-Test Strategies in Network Chip Architectures. France: Design And Reuse S.A; 2025.
15. Pillmeier MR. Barrel Shifter Design, Optimization, and Analysis. United States: Lehigh University; 2002.
16. Agrawal P, Mehra R. Design and performance analysis of barrel shifter using 45nm technology. IOSR J VLSI Signal Process 2016;6:38-44.
17. Maity NP, Maity R. FPGA implementation of 4-bit and 8-bit barrel shifters. Int J Electron Commun Technol 2013;4:45-7.
18. Patnaik S, Pandey S, Patil S. Design of various 4 bit shifters using CMOS 32nm technology. Int J Eng Res 2015;4:522-6.
19. Bhardwaj KK, Khare V. Design of shift invert coding using barrel shifter. Int J Pure Appl Math 2018;118:247-52.
20. Sachan P, Katiyar A, Didal A, Gautam P. Barrel shifter. Int J Sci Eng Technol 2014;2:1434-40.

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